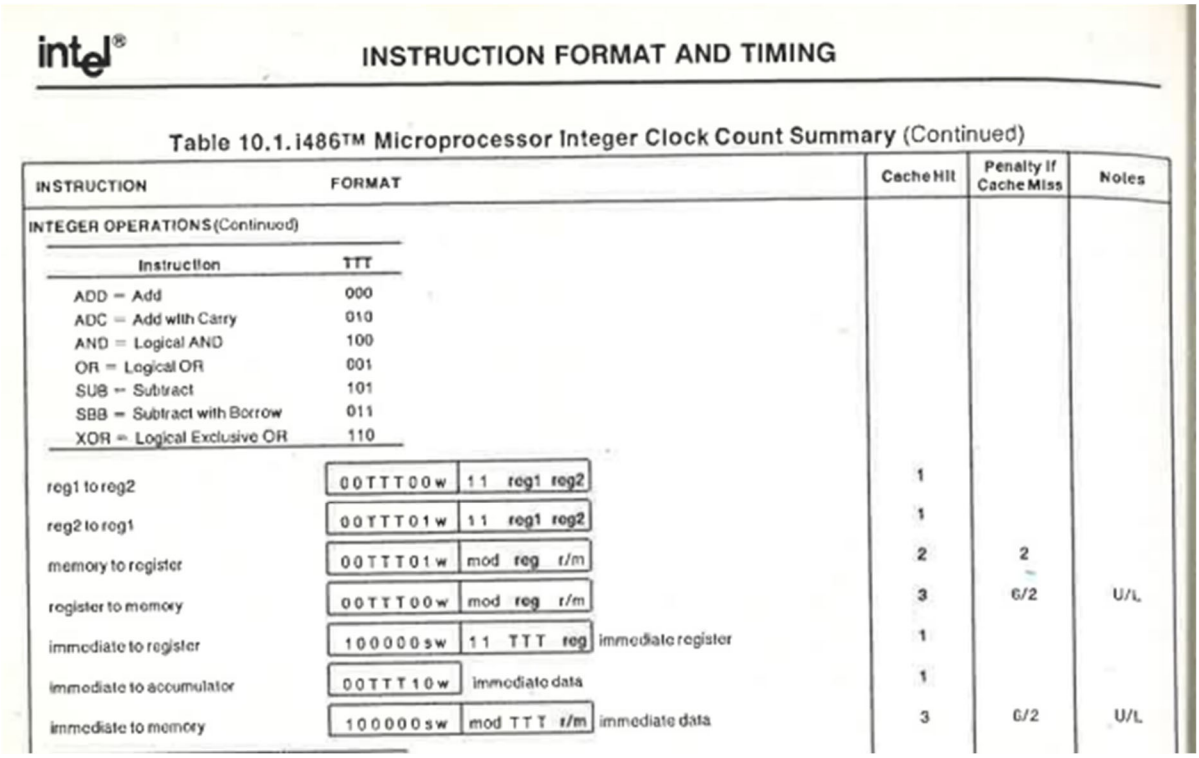
Intel 80486 introduced 1989, 33 MHz
1992, 66 MHz
1993, replaced by Pentium

int operations

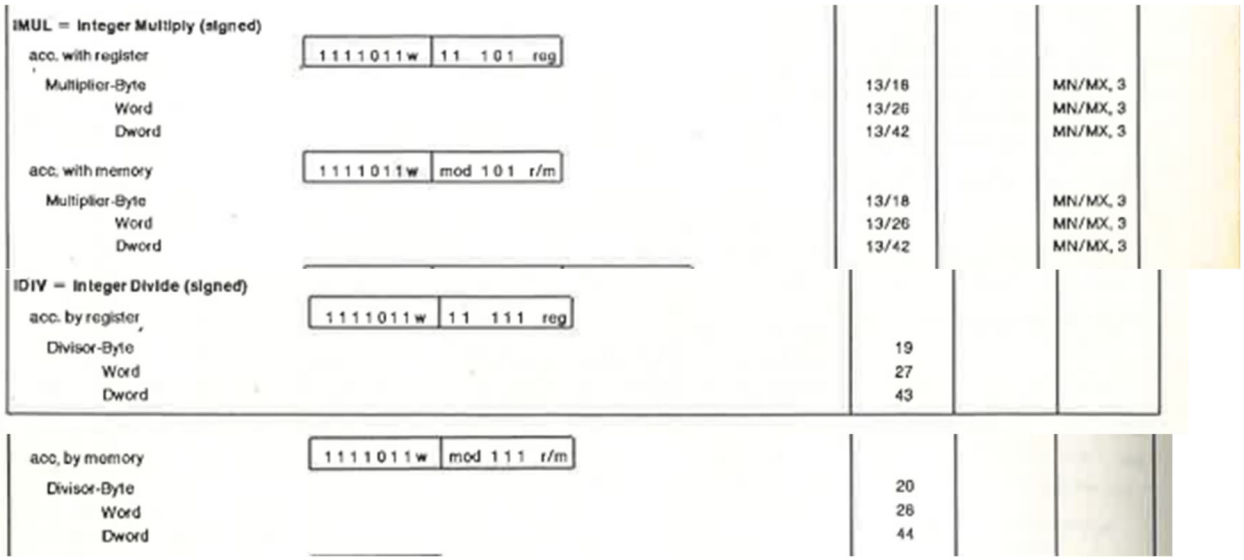


intel®

INSTRUCTION FORMAT AND TIMING

Table 10.1. i486™ Microprocessor Integer Clock Count Summary (Continued)

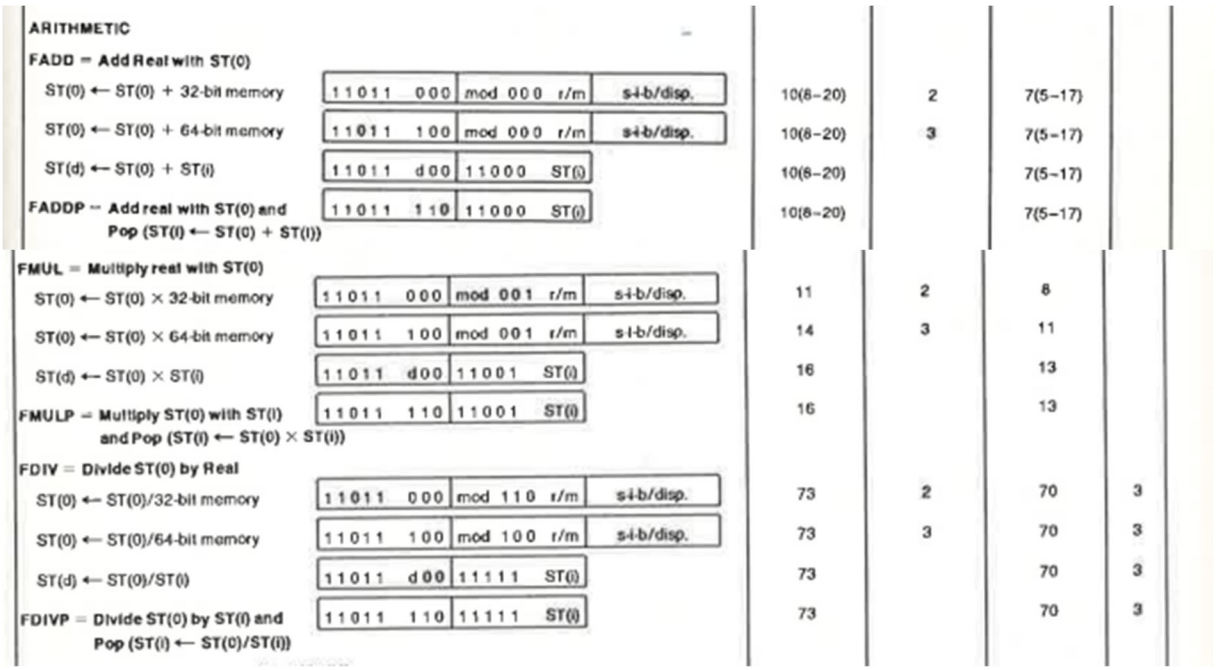
INSTRUCTION	FORMAT	Cache Hit	Penalty If Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
Instruction / TTT: ADD = Add 000; ADC = Add with Carry 010; AND = Logical AND 100; OR = Logical OR 001; SUB = Subtract 101; SBB = Subtract with Borrow 011; XOR = Logical Exclusive OR 110				
reg1 to reg2	00TTT00w 11 reg1 reg2	1		
reg2 to reg1	00TTT01w 11 reg1 reg2	1		
memory to register	00TTT01w mod reg r/m	2	2	
register to memory	00TTT00w mod reg r/m	3	6/2	U/L
immediate to register	100000sw 11 TTT reg immediate register	1		
immediate to accumulator	00TTT10w immediate data	1		
immediate to memory	100000sw mod TTT r/m immediate data	3	6/2	U/L



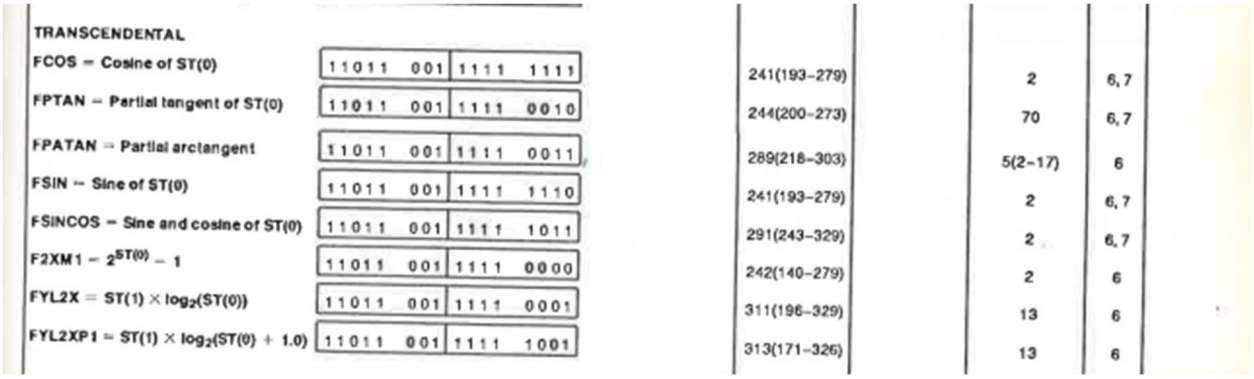
IMUL = Integer Multiply (signed)				
acc. with register	1111011w 11 101 reg			
Multiplier-Byte		13/18		MN/MX, 3
Word		13/26		MN/MX, 3
Dword		13/42		MN/MX, 3
acc. with memory	1111011w mod 101 r/m			
Multiplier-Byte		13/18		MN/MX, 3
Word		13/26		MN/MX, 3
Dword		13/42		MN/MX, 3
IDIV = Integer Divide (signed)				
acc. by register	1111011w 11 111 reg			
Divisor-Byte		19		
Word		27		
Dword		43		
acc. by memory	1111011w mod 111 r/m			
Divisor-Byte		20		
Word		28		
Dword		44		

At 33 MHz, 44 clocks = 1.33 micro-seconds

float and double operations



ARITHMETIC								
FADD = Add Real with ST(0)								
ST(0) ← ST(0) + 32-bit memory	11011 000	mod 000 r/m	s-i-b/disp.	10(8–20)	2	7(5–17)		
ST(0) ← ST(0) + 64-bit memory	11011 100	mod 000 r/m	s-i-b/disp.	10(8–20)	3	7(5–17)		
ST(d) ← ST(0) + ST(i)	11011 d00	11000 ST(i)		10(8–20)		7(5–17)		
FADDP = Add real with ST(0) and Pop (ST(i) ← ST(0) + ST(i))	11011 110	11000 ST(i)		10(8–20)		7(5–17)		
FMUL = Multiply real with ST(0)								
ST(0) ← ST(0) × 32-bit memory	11011 000	mod 001 r/m	s-i-b/disp.	11	2	8		
ST(0) ← ST(0) × 64-bit memory	11011 100	mod 001 r/m	s-i-b/disp.	14	3	11		
ST(d) ← ST(0) × ST(i)	11011 d00	11001 ST(i)		16		13		
FMULP = Multiply ST(0) with ST(i) and Pop (ST(i) ← ST(0) × ST(i))	11011 110	11001 ST(i)		16		13		
FDIV = Divide ST(0) by Real								
ST(0) ← ST(0)/32-bit memory	11011 000	mod 110 r/m	s-i-b/disp.	73	2	70	3	
ST(0) ← ST(0)/64-bit memory	11011 100	mod 100 r/m	s-i-b/disp.	73	3	70	3	
ST(d) ← ST(0)/ST(i)	11011 d00	11111 ST(i)		73		70	3	
FDIVP = Divide ST(0) by ST(i) and Pop (ST(i) ← ST(0)/ST(i))	11011 110	11111 ST(i)		73		70	3	



TRANSCENDENTAL						
FCOS = Cosine of ST(0)	11011 001	1111 1111	241(193–279)	2	6, 7	
FPTAN = Partial tangent of ST(0)	11011 001	1111 0010	244(200–273)	70	6, 7	
FPATAN = Partial arctangent	11011 001	1111 0011	289(218–303)	5(2–17)	6	
FSIN = Sine of ST(0)	11011 001	1111 1110	241(193–279)	2	6, 7	
FSINCOS = Sine and cosine of ST(0)	11011 001	1111 1011	291(243–329)	2	6, 7	
F2XM1 = $2^{ST(0)} - 1$	11011 001	1111 0000	242(140–279)	2	6	
FYL2X = ST(1) × $\log_2$(ST(0))	11011 001	1111 0001	311(196–329)	13	6	
FYL2XP1 = ST(1) × $\log_2$(ST(0) + 1.0)	11011 001	1111 1001	313(171–326)	13	6	

At 33 MHz, 73 clocks = 2.21 micro-seconds
241 clocks = 7.30 micro-seconds